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IN THE CLAIMS:

Please cancel claims 16-29.

Please amend the remaining claims as follows:

~~{e1}~~

1. (Currently Amended) A fin-type field effect transistor (FinFET) comprising:
 - a first fin having a central channel region and source and drain regions adjacent said channel region;
 - a gate structure intersecting said first fin and covering said channel region; and
 - a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure, and said channel region of said second fin is devoid of a connection to any source or drain regions.

~~{e2}~~

2. (Currently Amended) ~~The FinFET in claim 1,~~ A fin-type field effect transistor (FinFET) comprising:
 - a first fin having a central channel region and source and drain regions adjacent said channel region;
 - a gate structure intersecting said first fin and covering said channel region; and
 - a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure wherein said second fin has a length equal to a width of said gate structure.

~~{e3}~~

3. (Currently Amended) ~~The FinFET in claim 1,~~ A fin-type field effect transistor (FinFET) comprising:
 - a first fin having a central channel region and source and drain regions adjacent said channel region;
 - a gate structure intersecting said first fin and covering said channel region; and

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a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure, wherein said first fin is longer than said second fin.

~~[e4]~~

4. (Currently Amended) The FinFET in claim 1, wherein said source and drain regions of said first fin extend beyond said gate structure.

~~[e5]~~

5. (Currently Amended) ~~The FinFET in claim 1,~~ A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent said channel region;

a gate structure intersecting said first fin and covering said channel region; and

a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure, wherein said second fin does not extend beyond said gate structure.

~~[e6]~~

6. (Currently Amended) The FinFET in claim 1, further comprising source and drain contacts covering said source and drain regions of said first fin.

~~[e7]~~

7. (Currently Amended) The FinFET in claim 1, wherein no contacts are positioned adjacent said second fin.

~~[e8]~~

8. (Currently Amended) A fin-type field effect transistor (FinFET) comprising:
- a first fin having a central channel region and source and drain regions adjacent said channel region; and
 - a second fin consisting of a channel region, said channel region of said second fin is devoid of a connection to any source or drain regions.

~~[e9]~~

9. (Currently Amended) ~~The FinFET in claim 8~~ A fin-type field effect transistor (FinFET) comprising:
- a first fin having a central channel region and source and drain regions adjacent channel region; and
 - a second fin consisting of a said channel region, wherein said first fin is longer than said second fin.

~~[e10]~~

10. (Currently Amended) The FinFET in claim 8, further comprising a gate intersecting said first fin and covering said channel region.

~~[e11]~~

- ~~11. (Currently Amended) The FinFET in claim 10 A fin-type field effect transistor (FinFET) comprising:-~~
- a first fin having a central channel region and source and drain regions adjacent channel region; and

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a second fin consisting of a said channel region, wherein said second fin has a length equal to a width of said gate structure.

[e12]—

12. (Currently Amended) The FinFET in claim 10, wherein said source and drain regions of said first fin extend beyond said gate structure.

[e13]—

13. (Currently Amended) ~~The FinFET in claim 10~~ A fin-type field effect transistor (FinFET) comprising:

a first fin having a central channel region and source and drain regions adjacent channel region; and

a second fin consisting of a said channel region, wherein said second fin does not extend beyond said gate structure.

[e14]—

14. (Currently Amended) The FinFET in claim 8, further comprising source and drain contacts covering said source and drain regions of said first fin.

[e15]—

15. (Currently Amended) The FinFETs in claim 8, wherein no contacts are positioned adjacent said second fin.

16-29 (Cancelled).